FIGURE 1

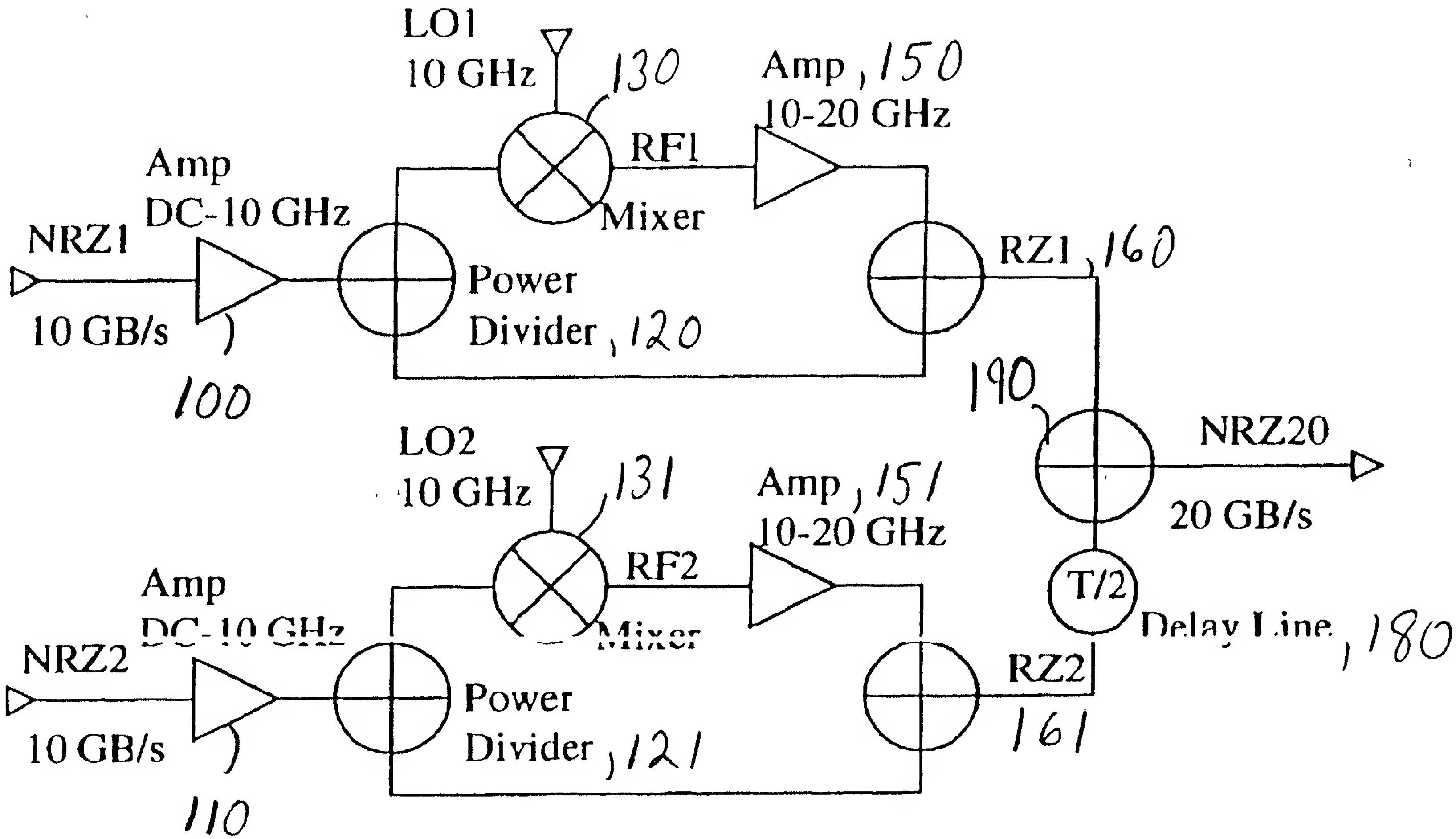

FIGURE 2

		Clock	
		1	0
Data	1	1	0
	0	0	0

- **Logic Diagram resulting from And gate**
- **Two output states**

FIGURE 3

		Clock	
		1	-1
Data	1	1	-1
	0	0	0

- **Logic diagram resulting from mixer**
- **Three output states**

- **Reduce to two states by adding original data stream**
- **Two output levels**
- **Effects NRZ to RZ conversion**

		Clock							
		1	-1						
Data	1	1	1	:	Data	1	=	1	0
	0	0	0			0		0	0

FIGURE 4